AN3024
Application note

SPC560B4x/5x, SPC560C4x/5x hardware design guideline

Introduction

This application note complements the information in the SPC560Bxx and SPC560Cxx device datasheet (see *Section Appendix A: Document management*) by describing requirements useful for a hardware implementation of the development board features such as power supply, reset control, clock management, boot mode setting, debug management and I/Os settings. It shows how to use the product and defines the minimum hardware resources required to start an application development.

Sections of this document describe certain device features in brief without describing the device blocks in detail. For a detailed description of these features, refer to the device datasheet, the reference manual *RM0017* or the SPC560Bxx and SPC560Cxx errata sheet, or all three documents (see *Section A.1: Reference documents*).

This application note applies to the SPC560Bxx and SPC560Cxx devices listed in *Table 1*.

Table 1. Device summary

Reference	Part number
SPC560B4x	SPC560B40L3, SPC560B40L5, SPC560B44L3
SPC560B5x	SPC560B50L3, SPC560B50L5, SPC560B50B2
SPC560C4x	SPC560C40L3, SPC560C44L3
SPC560C5x	SPC560C50L3

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1 Power supplies

1.1 Introduction

The device requires a 3.3 V or 5.0 V operating voltage supply (high voltage). An embedded regulator is used to supply the internal 1.2 V digital power (low voltage).

Three different high voltage pin supply types are used:

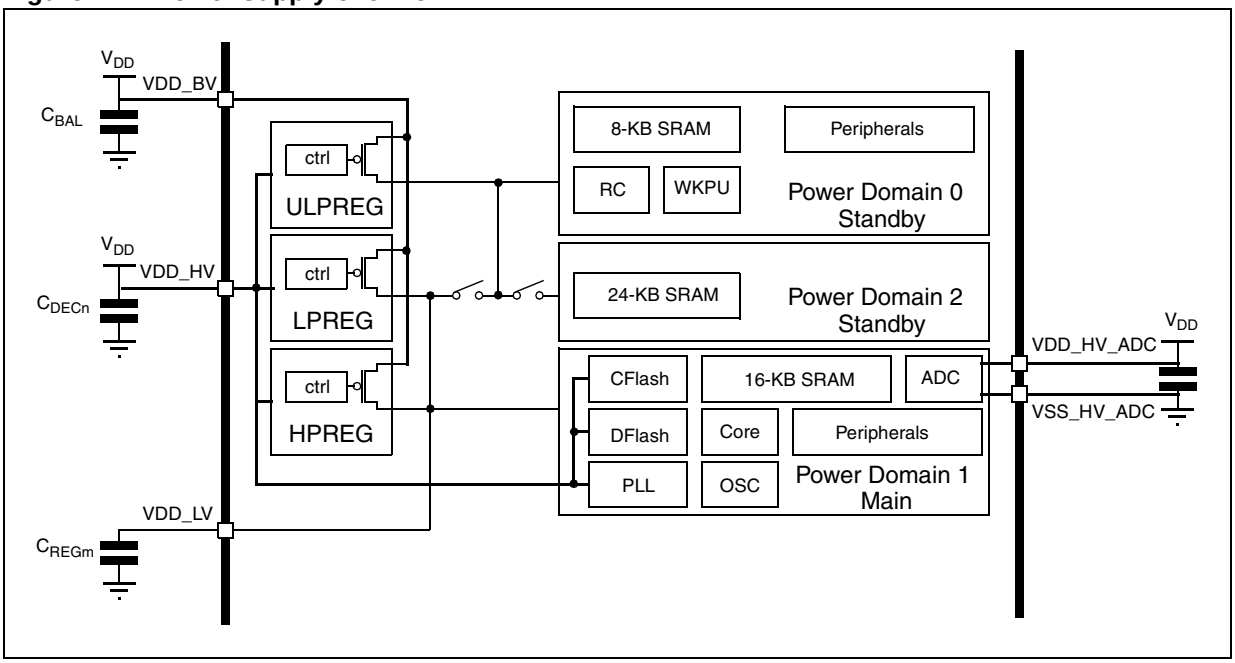
- VDD_HV—high voltage external power supply for internal voltage regulators, I/O pins and Flash
- VDD_BV—high voltage external power supply for internal voltage regulator ballast transistors
- VDD_HV_ADC—high voltage external power supply for analog-to-digital converter

Three different independent voltage regulators provide the 1.2 V digital power supply:

- HPREG—high power internal voltage regulator used during normal operations. It can be switched off in STOP mode and is automatically switched off in STANDBY mode.
- LPREG—low power internal voltage regulator used when HPREG is off. It can be switched off in STOP mode and is automatically switched off in STANDBY mode.
- ULPREG—ultra low power internal voltage regulator. Always switched on and used in STANDBY or in STOP mode when all other regulators are switched off.

External capacitors connected between the VDD_LV/VSS_LV pin pairs ensure the stability of the internal 1.2 V HPREG and LPREG regulators.

Figure 1. Power supply overview



For a detailed list of supply-related pins for all packages, please refer to the voltage supply pins section in *RM0017* (see *Section A.1: Reference document*).

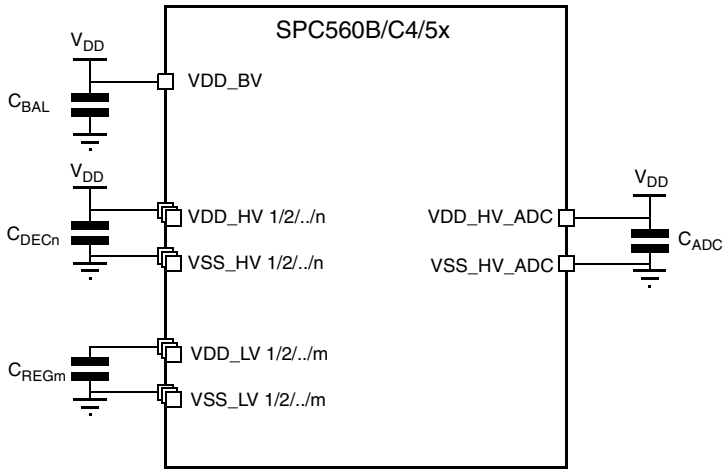
1.2 Power supply scheme

The circuit is powered by a stabilized power supply V_{DD}.

- VDD_HV pins must be connected to V_{DD} with external decoupling capacitors C_{DECn}.
- VDD_BV pin must be connected to V_{DD} with external decoupling capacitor C_{BAL}.
- VDD_HV_ADC pin be connected to V_{DD} with external decoupling capacitor C_{ADC}.
- VDD_LV pins must be connected with external decoupling capacitors C_{REGm} placed as close as possible to the device pins.
- VSS_HV and VSS_LV pins must all be connected together to GND.

Refer to the voltage regulator electrical characteristics section in the device datasheet (see *Section A.1: Reference document*) for exact capacitor values.

Figure 2. Power supply scheme



Note:
The device cannot be supplied with external 1.2 V. The on-chip regulator must **always** be used.

Caution: All BV and HV and ADC supplies must be powered with a voltage level in the range $V_{DD} \pm 0.1$ V, and all grounds must be in the range $V_{SS} \pm 0.1$ V.

1.3 Current consumption and voltage regulator

In order to select a suitable external voltage regulator and design a supply circuit, the designer of the application must consider:

1. The maximum consumption in steady state
2. The maximum inrush current during device start-up

The maximum consumption in steady state depends on the frequency of the CPU, the usage of the peripheral and the current drawn by the outputs. It can be estimated by referring to the device datasheet (see *Section A.1: Reference document*).

The inrush current required by the device during power-on reset or exit from STANDBY is clamped at 400 mA and lasts for few microseconds (maximum 20 µs) until the C_{REGm} stabilization capacitors (total value ~1 µF) are charged. This current is drawn from the VDD_BV pin.

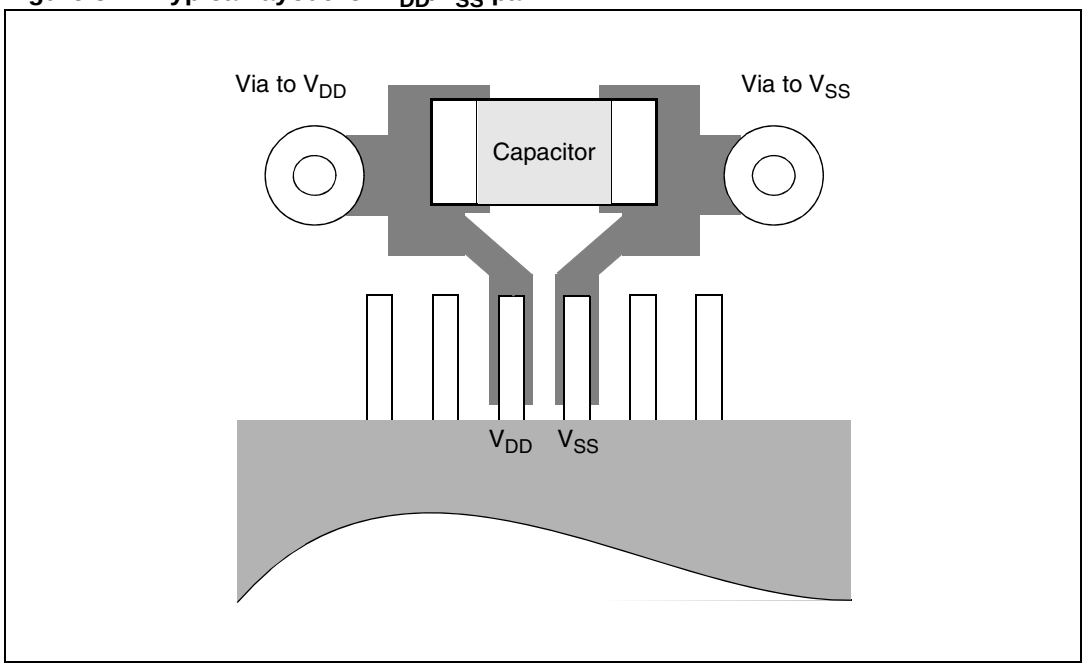
Note: The inrush current must be considered to dimension the decoupling capacitance of the ballast (C_DEC1) value as during this inrush the application must ensure V_{DD} remains in the voltage range of the application (5 V or 3.3 V ±10 %). The steady current is used to define the voltage regulator capability of the application.

1.4 Layout recommendations

All the supply connections, including pads, tracks and vias, must have impedance as low as possible (less than 5 nH). This is typically achieved by using thick and wide Cu tracks and preferably dedicated power supply planes in multilayer PCBs.

Moreover, it is recommended to use both low equivalent series resistance (ESR) and low equivalent series inductance (ESL) capacitors. The capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. *Figure 3* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 3. Typical layout for V_{DD}/V_{SS} pair



2 Reset

2.1 Introduction

The device has an integrated POR (power-on reset) to ensure a correct power-up sequence: The device remains in reset state as long as the V_{DD} is below the specified threshold.

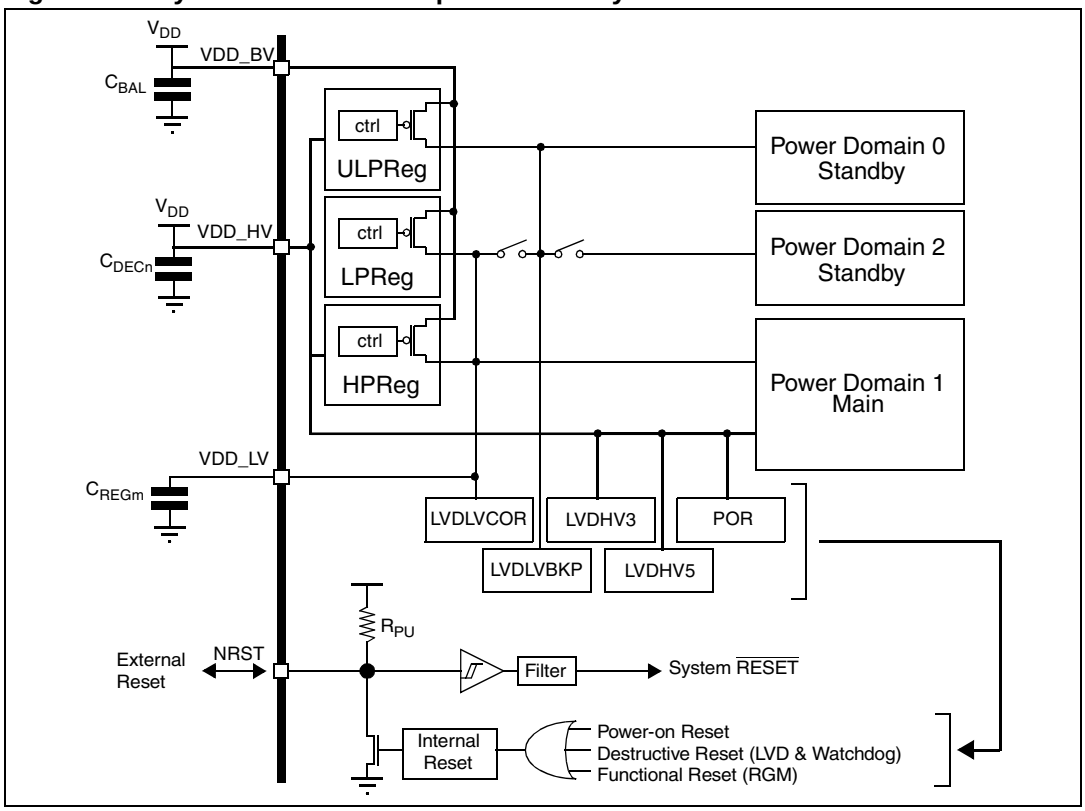
The device has four low voltage detectors to monitor V_{DD_HV} and V_{DD_LV}:

- LVDHV3—monitors V_{DD} so as to ensure that the device reset occurs for voltage values less than minimum functional supply value
- LVDHV5—monitors V_{DD} when the application uses devices operating in the range 5.0 V ± 10%. By default the LVDHV5 is disabled (to allow 3.3 V operation) and must be activated by the application.
- LVDLVCOR—monitors the voltage provided to the main power domain (core, Flash, PLL, JTAG and peripherals not included in the standby power domain)
- LVDLVBKP—monitors the voltage provided to the power domain in standby mode (8 Kbyte SRAM, optionally 24 Kbyte SRAM, power control unit, reset generation module, voltage regulator, wake-up unit, API, CAN sampler, internal RC oscillators, etc.)

The device has a dedicated bidirectional $\overline{\text{RESET}}$ pin (NRST) with Schmitt-Trigger characteristics and noise filter for system reset.

For detailed information on reset sequence, please refer to the reset state machine section in *RM0017* (see *Section A.1: Reference document*).

Figure 4. System reset and low power circuitry



2.2 Power-on reset (POR) and low voltage detectors (LVDs)

POR is required to initialize the chip during power-up and works only on the rising edge of the VDD_HV supply. It is asserted when V_{DD_HV} is above $V_{PORUPmin}$ and released when V_{DD_HV} is above V_{PORH}.

Once the POR is released, power management modules, including internal LVDs, are up and running. The system remains in reset state until the LVDHV3, LVDLVCOR and LVDLVBKP thresholds are reached.

Note: At power-up, although the V_{DD} slope at the VDD_HV pad rises, it must remain in the range of 3 V/s to 0.25 V/µs (see T_{VDD} parameter in the device datasheet*—refer to Section A.1: Reference document*).

2.3 System reset pin

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin (NRST) with Schmitt-Trigger characteristics and noise filter.

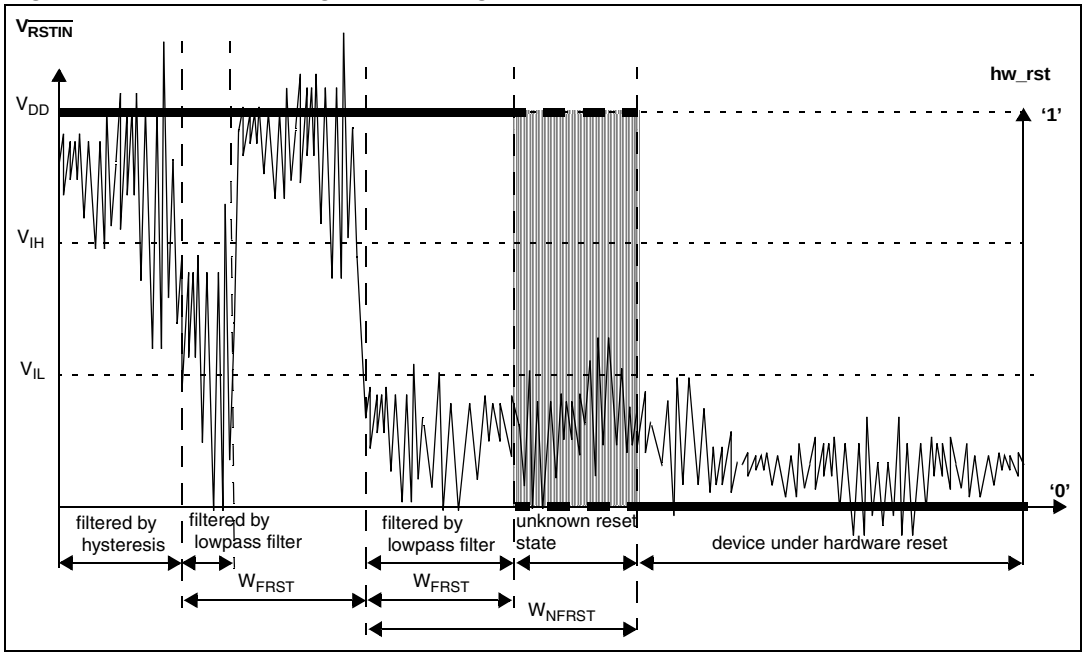
2.3.1 Input characteristics

The external reset signal (pulse) on the NRST pin must be greater than W_{NFRST} (500 ns). Pulses less than W_{FRST} (50 ns) are ignored. Any pulse between W_{FRST} and W_{NFRST} may or may not generate an internal reset.

A noise applied on the reset signal might wrongly put the device in reset. In order to avoid unexpected reset of the device, the NRST pad includes an analog filter which makes the system immune to noise.

For additional information about filter characteristics, please refer to the nRSTIN electrical characteristics section in the device datasheet (see *Section A.1: Reference document*).

Figure 5. Noise filtering on reset signal



2.3.2 Output characteristics

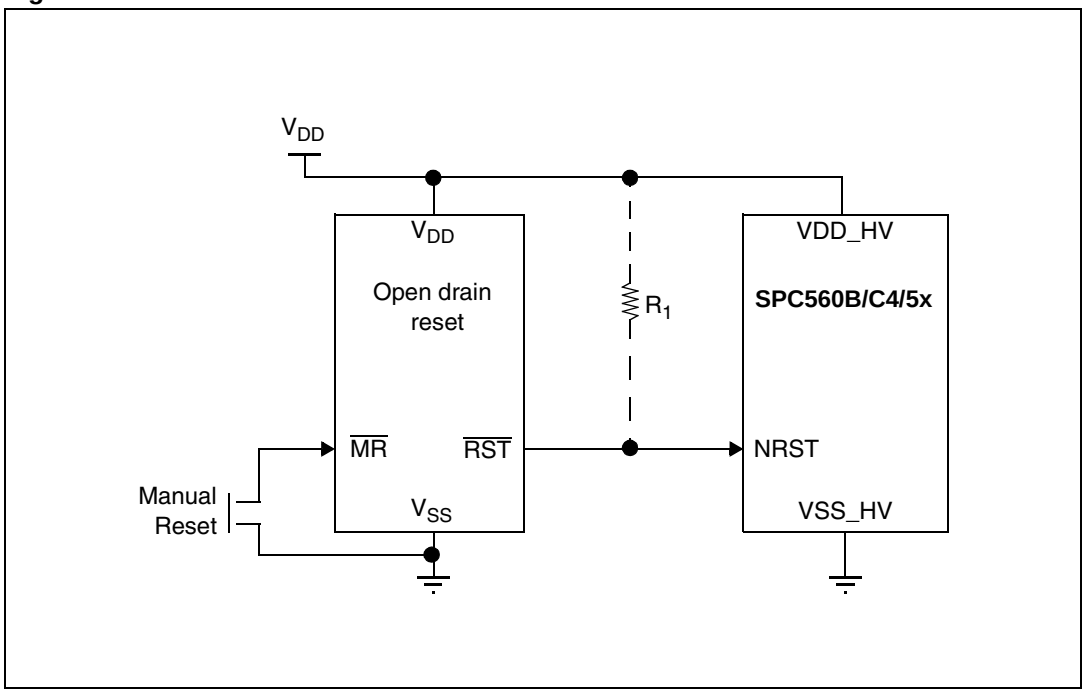
The NRST pad, when used as output, behaves as a MEDIUM pad (see the nRSTIN electrical characteristics section in the device datasheet—refer to *Section A.1: Reference document*).

The duration of the NRST active time depends on the reset source and the device configuration, but the minimum reset duration guaranteed is 80 µs.

2.4 Reset scheme

Figure 6 shows a typical circuit for controlling the NRST pin operation. The reset input pin has an internal weak pull-up configured by default exiting from power-on, thus R_1 can be omitted. In the case in which an external capacitor is used to filter the NRST external signal, an external pull-up reduces the charging time of this capacitor.

Figure 6. Reference reset circuit



3 ADC

3.1 Introduction

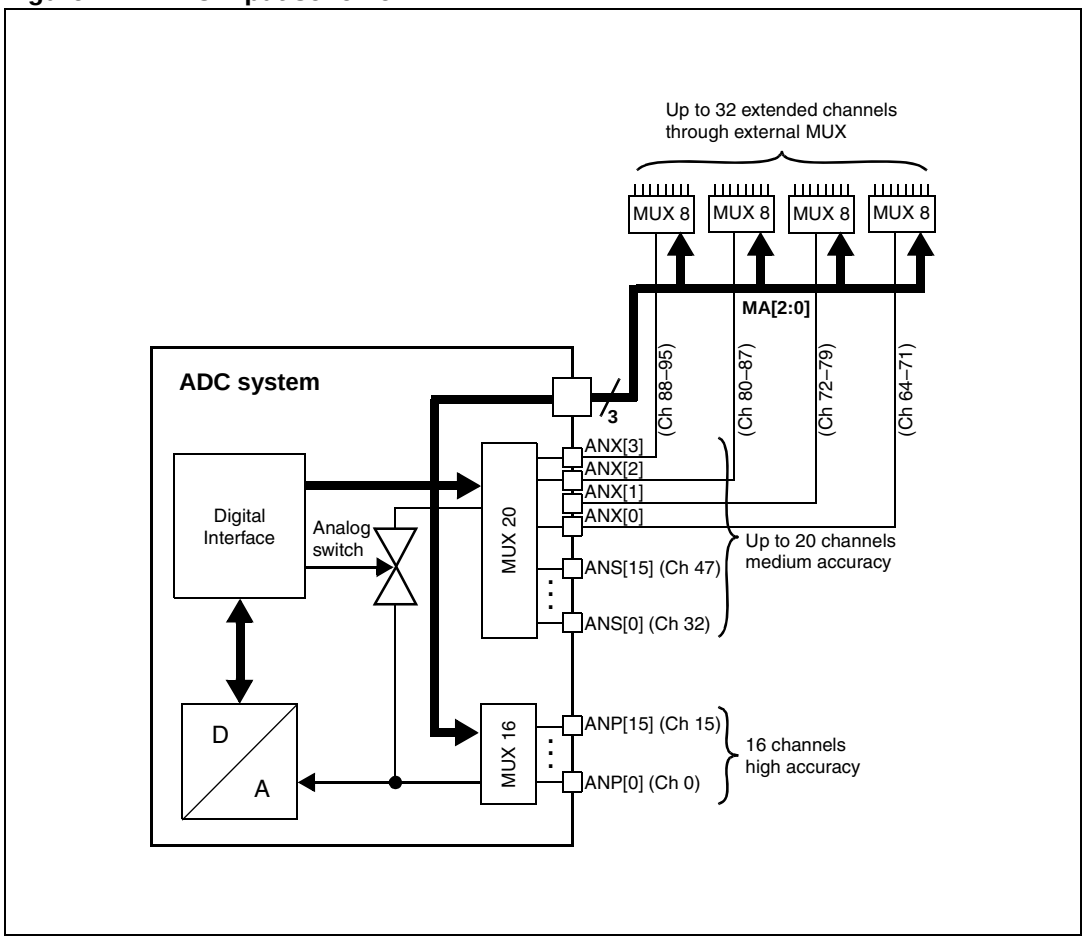
The device uses a dedicated supply pair VDD_HV_ADC/VSS_HV_ADC for the ADC analog module so as to decouple the ADC reference voltage from the noise generated either by another part of the device or by the external application components. VDD_HV_ADC must be at the same voltage level as the VDD_HV.

There are three different ADC input channels types:

- ANP—internal multiplexed precise channels used for conversion requiring a low TUE
- ANS—internal multiplexed standard channels used for conversion requiring a standard TUE
- ANX—external multiplexed channels used in conjunction with external multiplexer controlled directly by the device

ANPs are input only pins. For channel characteristics, please refer to the ADC electrical characteristics section in the device datasheet (see *Section A.1: Reference document*).

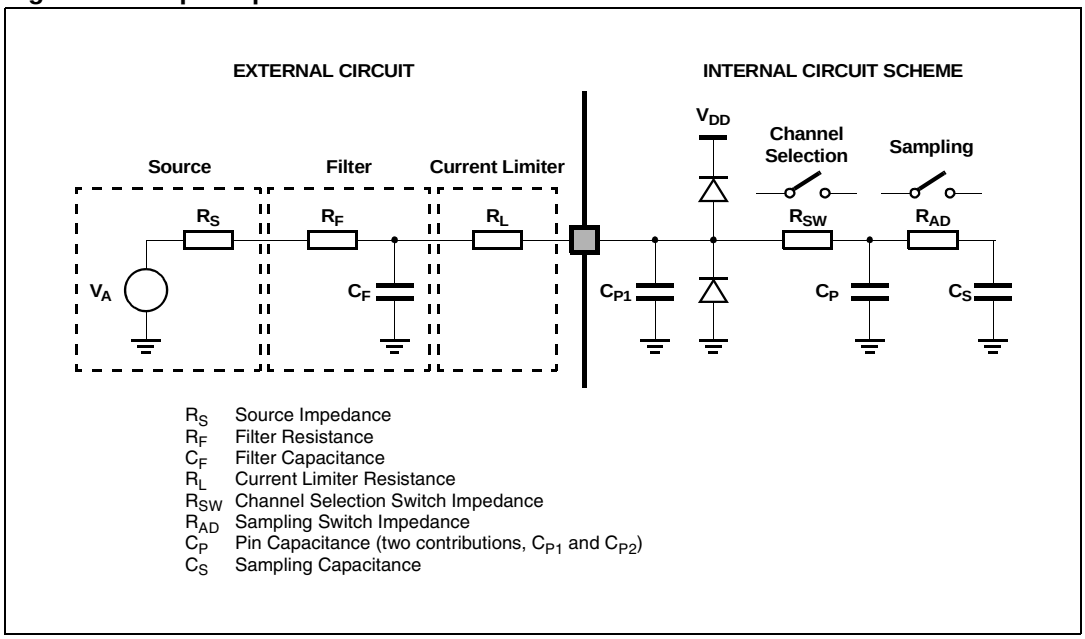
Figure 7. ADC input scheme



3.2 ADC performances optimization

The equivalent analog input interface of an ADC channel is shown in *Figure 8*.

Figure 8. Input equivalent circuit



To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the *Equation 1*:

Equation 1

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}LSB$$

Please refer to the analog-to-digital converter (ADC) chapter in *RM0017* for type specification versus pins and to the ADC electrical characteristics section in the device datasheet for parameter values (see *Section A.1: Reference document*).

4 External oscillators

4.1 Introduction

The product offers four clock sources to cover the various types of application:

- Fast internal RC oscillator
- Fast external crystal oscillator
- Slow internal RC oscillator
- Slow external crystal oscillator

An internal PLL is available to optimize the oscillator choice versus the required system frequency.

This section is focused on the two external oscillators:

- The fast external crystal oscillator for the system clock covering 4 MHz to 16 MHz
- The slow external crystal oscillator for the 32 kHz low power clock

4.2 Fast external crystal oscillator (4 to 16 MHz)

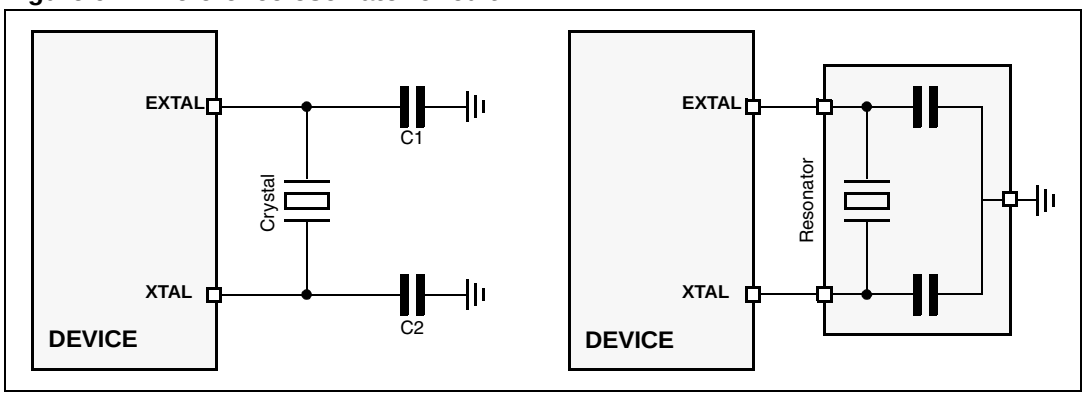
The fast external crystal oscillator must be in the frequency range from 4 MHz to 16 MHz. If the crystal (resonator) is in the range from 4 MHz to 8 MHz, the oscillator margin can be adjusted by using an option bit which reduces the fast external crystal oscillator consumption (low consumption configuration). The default manufacturing oscillator margin is in the range from 4 MHz to 16 MHz.

Please refer to the *RM0017* (see *Section A.1: Reference document*) for additional information about option bits and oscillator margin.

To reduce EMC emissions, it is recommended to use the slowest crystal (resonator) together with the internal PLL, thus achieving the proper system operating frequency. The drawback of using a slow crystal is the longer start-up time.

Figure 9 shows the external circuit needed for using the oscillator with a crystal or a resonator.

Figure 9. Reference oscillator circuit

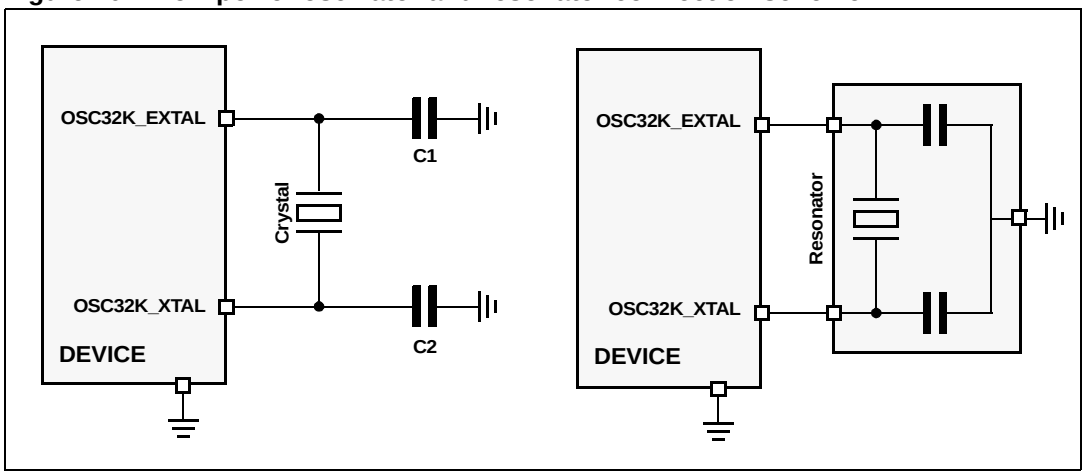


For additional information, please refer to the fast external crystal oscillator (4 to 16 MHz) electrical characteristics section in the device datasheet (see *Section A.1: Reference document*).

4.3 Slow external crystal oscillator (32 kHz)

Figure 10 shows the external circuit needed for using the low power oscillator with a 32 kHz crystal.

Figure 10. Low power oscillator and resonator connection scheme



For additional information, please refer to the slow external crystal oscillator (32 kHz) electrical characteristics section in the device datasheet (see *Section A.1: Reference document*).

4.3.1 Some recommended crystal

Table 2 gives the references of recommended crystals certified by resonators suppliers and verified through designer simulation in addition to the ones listed in the DS..

Table 2. Recomanded crystal

Part number	Family name	Freq.	CL	Supplier
EXS00A-MU00265	NX3215SA	32kHz	15pF	NDK
1TJF0SPFP1AC00E	DST310S	32kHz	15pF	KDS

However it is suggested to perform matching directly on customer application board, in order to verify board parassitics.

4.4 Layout recommendations

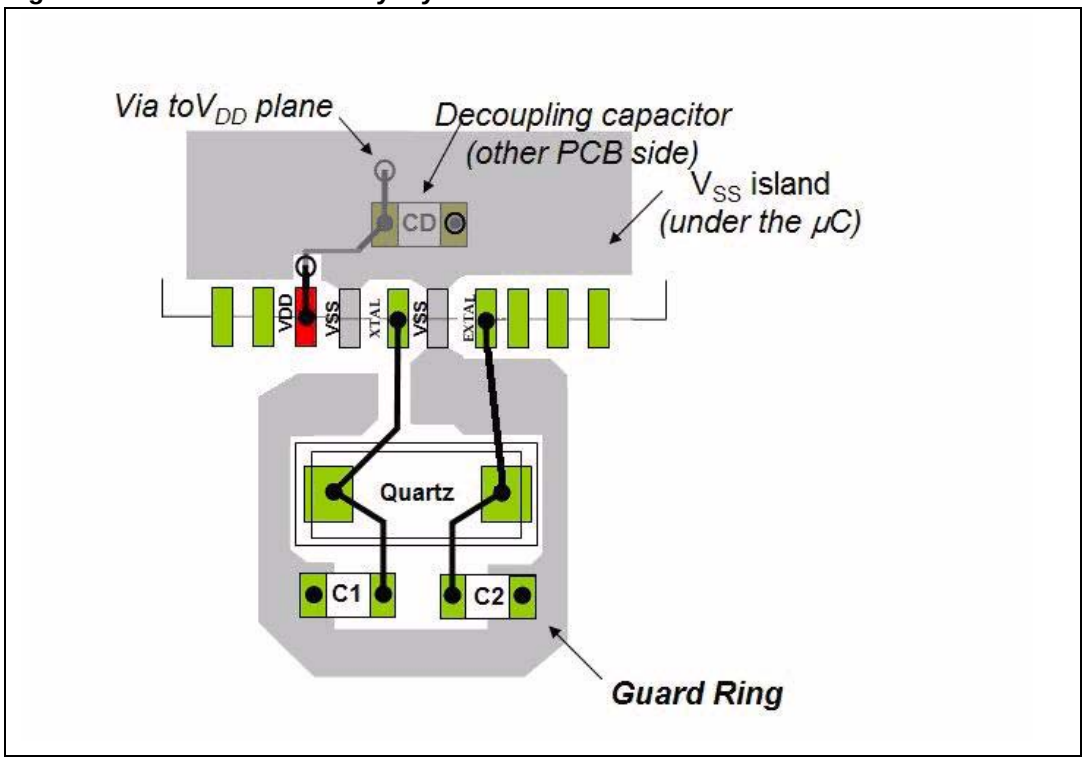
The following recommendations should be observed for designing the oscillator circuitry layout:

- A current flow at the crystal fundamental frequency runs through the oscillator circuit. If the oscillator is clipped, then the higher order harmonics are present. To minimize the emissions generated by these currents, the oscillator circuit should be kept as compact as possible.
- VSS_HV should be connected directly to GND (V_{SS} island) so that return currents can flow easily between VSS_HV and the two capacitors (C_1 and C_2).
- Avoid other high frequency signals near the oscillator circuitry.

- Use the same GND for oscillator and oscillator driver (VSS_HV is between EXTAL and XTAL, V_{SS} island)
- Layout: configure the GND supply at low impedance.
- Shield the crystal with an additional ground plane underneath the crystal.
- Do not place sensitive signals near the oscillator. Analyze cross-talk between different layers.
- The VSS pins close to the XTAL pin must be connected to GND plane (V_{SS} island) and decoupled from the closest VDD pin.
- Capacitors are placed between both ends of the crystal and GND (guard ring). The ring must be as small as possible.
- If the crystal package is metallic, it should be connected directly to GND.
- For isolating the noise from or to a particular area of the PCB, it is possible to surround this area with a “guard ring.”

Figure 11 shows an example of an oscillator circuitry layout.

Figure 11. Oscillator circuitry layout



5 Boot configuration

5.1 Introduction

The boot of the device is managed by the boot assist module (BAM).

The following boot modes are supported:

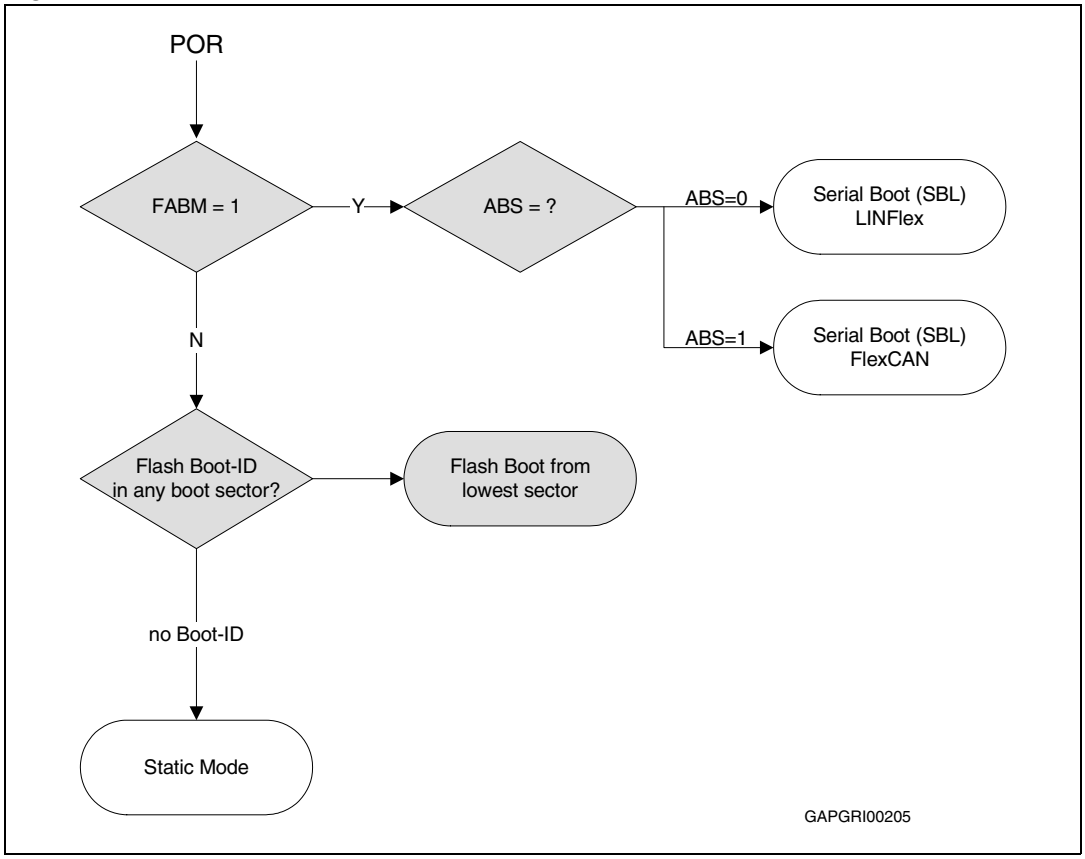
- Single chip (SC)—The device boots from the first bootable section of the Flash main array.
- Serial boot (SBL)—The device downloads boot code from either LINFlex_0 or FlexCAN_0 interface and executes it.

The boot mode selection is obtained by setting two pins: FAB and ABS[0].

5.2 Boot mode selection

The device detects the boot mode based on external pins (FAB and ABS[0]) and device status. *Figure 12* shows the boot sequence.

Figure 12. Boot mode selection



In *Figure 12*, the grey blocks represent hardware-implemented functions, while the white ones are software-implemented functions in ROM memory.

To boot either from FlexCAN_0 or LINFlex_0, the device must be forced into an alternate boot loader mode via FAB pin (pad PA[9]). The type of alternate boot mode (CAN or LIN) is selected according to the ABS[0] pin (pad PA[8]).

FAB and ABS[0] pins must be forced in the required state before initiating the reset sequence.

Table 3. Boot mode selection

FAB (pad PA[9])	ABS[0] (pad PA[8])	Boot ID	Boot mode
1	0	X	LINFlex_0
1	1	X	FlexCAN_0
0	X	Valid	Single chip
0	X	Not valid	Static mode

In single-chip mode, hardware searches the Flash boot sector for a valid boot ID. As soon as the device detects a bootable sector, it reads the 32-bit word at offset 0x4 at the detected sector. Single-chip mode is managed by hardware and BAM is not used.

BAM is executed only in the following cases:

- Serial boot mode has been selected by FAB pin.
- Hardware has not found a valid Boot-ID in any Flash boot locations.

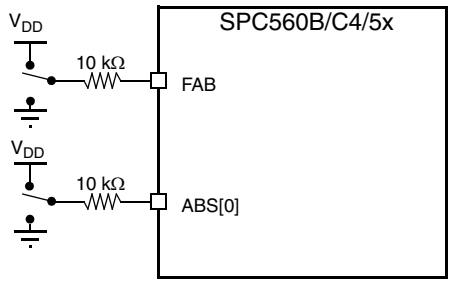
If booting is not possible with the selected configuration (for example, if no Boot ID is found in the selected boot location) then the device enters the static mode.

Please refer to the boot assist module (BAM) chapter in *RM0017* (see *Section A.1: Reference document*) for additional information.

5.3 Boot pin scheme

To make all boot configurations possible, it is recommended to use external switches connected to the FAB and ABS[0] pins, as shown in *Figure 13*.

Figure 13. Boot mode selection implementation example



Note: The pins FAB and ABS[0] have the boot mode selection function during reset phase. After reset phase, they are normal I/O pins and can be used according to application needs.

GAPGRI00206

6 Debug

6.1 Introduction

The device features JTAG and Nexus 2+ interfaces.

The Nexus 2+ interface is available only on the LBGA208 development package and is not discussed in this document. Nexus 2+ pins are located on dedicated pads.

6.2 JTAG I/Os

The JTAG interface is composed of:

- Test data input (TDI) on pin PC[0]
- Test data output (TDO) on pin PC[1]
- Test mode select (TMS) on pin PH[10]
- Test clock input (TCK) on pin PH[9]

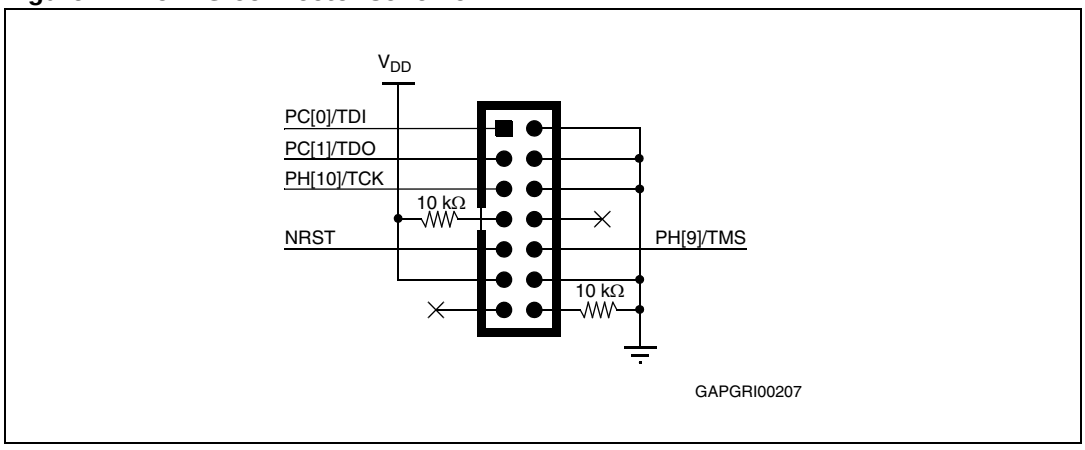
Out of reset, all JTAG signals are configured for the JTAG communication. They can be configured by software as user I/Os and made available to the application. If the application needs to combine both the JTAG functionality for debug and programming purposes together with the standard I/O function, some limitations must be considered:

- PC[0], PC[1], PH[9] and PH[10] cannot be debugged using a JTAG debug interface.
- The configuration of PC[0], PC[1], PH[9] or PH[10] as user I/Os prevents the communication with the debugger, making impossible to debug the application.
- These pins can only be set back to the JTAG functionality by means of a hardware or software reset (it cannot be done through the JTAG debugger).

An external hardware application connected to those signals might interfere with JTAG signals, making it impossible to enter debug mode without disconnecting the external hardware. It is preferable to use these JTAG pins to define the hardware configuration of the application rather than critical application functions.

6.3 JTAG connector scheme

Figure 14. JTAG connector scheme



7 I/Os

7.1 Introduction

The device features a unique pad technology to sustain a current injection of ± 5 mA on digital and analog inputs. A simple serial resistor is sufficient to protect the input characteristics.

7.2 I/O types

The device features three I/O types with different drive strength:

- SLOW type—This is the most common output type suitable for most of the application output signals and ensuring low electromagnetic emission.
  It allows to drive up to 2 mA and can sustain a maximum frequency of 2 MHz.
- MEDIUM type—This output type can sustain a higher frequency with a reduced delay to meet the requirements of SPI communication or high speed CAN communication.
  It allows to drive up to 3.8 mA and can sustain a maximum frequency of 16 MHz.
  Out of reset, the medium speed outputs are configured as slow. To obtain the medium performance the application must configure the slew rate using the SRC field in the corresponding SIUL pad configuration register (SIUL_PCR).
- FAST type—Only the Nexus MCKO signal features a fast pad which is not a user signal.

Maximum output frequency depends directly on the capacitive load connected on the output.

Please refer to the device datasheet and *RM0017* (see *Section A.1: Reference document*), for the detailed electrical characteristics and port mapping.

Note: 1 All output types have a slope control (current) to reduce the EMI.

2 TDO pad is medium speed only. Writing the SRC field in the corresponding SIUL_PCR has no effect.

7.3 I/Os configuration after reset

To avoid activating external components while under reset, all pads are forced to high impedance inputs, with the following exceptions:

- RESET is driven low
- Boot mode pins
  - FAB is pull-down
  - ABS[0] is pull-up
- JTAG pins
  - TCK, TMS and TDI are pull-up
  - TDO is high impedance

7.4 Maximum output current

The application must not modify the maximum current drive expected on each I/O type and I/O segment. An I/O segment is a group of pads supplied by the same V_{DD_HV}/V_{SS_HV} pair.

Table 4. I/O supply segment

Package	Supply segment					
	1	2	3	4	5	6
LBGA208(1)	Equivalent to LQFP144 segment pad distribution				MCKO	MDOn/MSEO
LQFP144	pin20–pin49	pin51–pin99	pin100–pin122	pin123–pin19	—	—
LQFP100	pin16–pin35	pin37–pin69	pin70–pin83	pin84–pin15	—	—

1. LBGA208 available only as development package for Nexus2+.

In order to keep the maximum current on each segment in specification, both static and dynamic consumptions must be considered:

- The maximum static current must remain below maximum I_{AVGSEG} value so as to ensure device reliability. The parameter I_{AVGSEG} represents the average current drawn by all outputs belonging to the same segment. For example, if V_{DD} = 5 V then I_{AVGSEG} = 70 mA.
- The maximum dynamic current must remain below maximum I_{DYNSEG} value so as to ensure the device functionality. The parameter I_{DYNSEG} represents the sum of the dynamic and static current drawn by all outputs belonging to the same segment. For example, if V_{DD} = 5 V then I_{DYNSEG} = 110 mA.

Please refer to the I/O pad current specification section in the device datasheet and *RM0017* (see *Section A.1: Reference document*) for the detailed electrical characteristics and port mapping.

The dynamic consumption is caused by the output driver transistors during the output switch and therefore is present only during the transition phase of the output (rising or falling edge).

For example, if the maximum dynamic consumption of a SLOW type output is 20 mA, the transition lasts for 50 ns. Moreover, supposing that there is no static consumption on this I/O segment a maximum of five slow type outputs can switch simultaneously (in this case, 50 ns) in order to respect the maximum I_{DYNSEG} expected value, I_{DYNSEG} = 110 mA.

If a static current is drawn from the same segment, the dynamic consumption must be reduced accordingly. For example, if 16 outputs of the same segment draw out a total static current equal to 25 mA, the maximum dynamic consumption is reduced to 85 mA.

7.5 I/O characteristic in STANDBY mode

In STANDBY mode the I/Os are disconnected from supply and they are in high impedance state. Only the wake-up lines can be configured as:

- High-impedance input (default configuration)
- Input with weak pull-up

The configuration of the wake-up lines is supported in the wake-up unit. Please refer to the wakeup unit (WKPU) chapter in *RM0017* (see *Section A.1: Reference document*) for additional information.

Note: All wake-up lines left floating cause additional consumption due to their Schmitt Trigger logic. To avoid unnecessary consumption all wake-up lines should be kept to V_{SS} or V_{DD} either by the application or using the internal weak pull-up.

The TDO pad is part of the STANDBY domain in order to provide a handshaking mechanism with a debugger in STANDBY mode. However, in STANDBY mode the TDO pin is configured as input without pull-resistor and as a consequence, when no debugger is connected, the TDO pad is floating causing additional current consumption.

In order to avoid additional consumption, TDO must be tied to V_{DD} or GND by means of an external pull-up (or pull-down) resistor in the range of 47–100 kΩ.

If the PA[1] pin is configured as NMI the pull-up is automatically activated, but this has no effect during STANDBY mode. In this case pull-up is then correctly configured through the WKPU_WIPUER register; no external resistor is necessary.

7.6 General consideration for I/O

To avoid excess consumption and to improve the reliability of the application it is recommended to configure unused I/Os as input with pull-up.

During the application design the absolute maximum voltage on I/O must be considered:

- respect to ground: +6 V
- respect to V_{DD}: Voltage of each pin must remain in the range from V_{DD} – 0.3 and V_{DD} + 0.3

For more details refer to the device datasheet (see *Section A.1: Reference document*).

8 EMC guidelines

This section summarizes recommendations for the system designers to improve the EMC (electromagnetic compatibility) and, in particular, to reduce the radiant emissions of a system based on the SPC560Bxx and SPC560Cxx devices.

Obviously, not all EMC techniques are covered. Therefore, it is recommended to refer to other, more general EMC documentation in parallel to the present application note.

8.1 SPC560Bxx/Cxx software configurations

The SPC560Bxx/Cxx family offers some features that allow, with software configurations, to cover some requests for reduction in the electromagnetic interference (or EMI) emissions:

- The system clock should be chosen to avoid overlapping with known frequency (bands of interest)
- The FMPLL gives the possibility to modulate the system clock so to reduce the picks of emission.
- Choose the lowest possible slew rate of pins accordantly with the functionality choose for the pins
- The peripherals that are not used in the application should be disabled and clock gated
- Configuring the unused pins as input weak pull-up (default configuration)

8.2 Hardware guidelines

Some recommendations to design a system layout are listed below:

- V_{DD} decoupling capacitors

  Decoupling capacitors must be used to decouple BV and all HV and ADC supply pins from GND. To avoid that the decoupling capacitors' parasitic inductance couples with the capacitance plane of the supply planes, certain measures of precaution should be taken:

  – Place the capacitors as close as possible to the V_{DD} pins on the SPC560Bxx/Cxx device.

  – Use power planes or wide traces to connect from the SPC560Bxx/Cxx device to the capacitor.

  – Use as many vias as possible in the connections from the SPC560Bxx/Cxx device to the capacitors. For example, use at least two vias to connect the positive side of the capacitor to the power plane.

- Fast external crystal oscillator

  To reduce EMC emissions, it is recommended to use the slowest crystal (resonator) together with the internal PLL, thus achieving the proper system operating frequency. The drawback of using a slow crystal is the longer startup time. In order to minimize the amount of emissions, generated from the currents flowing in the oscillator circuit at the crystal's fundamental frequency, the oscillator circuit should be kept as compact as possible.

- Grounding

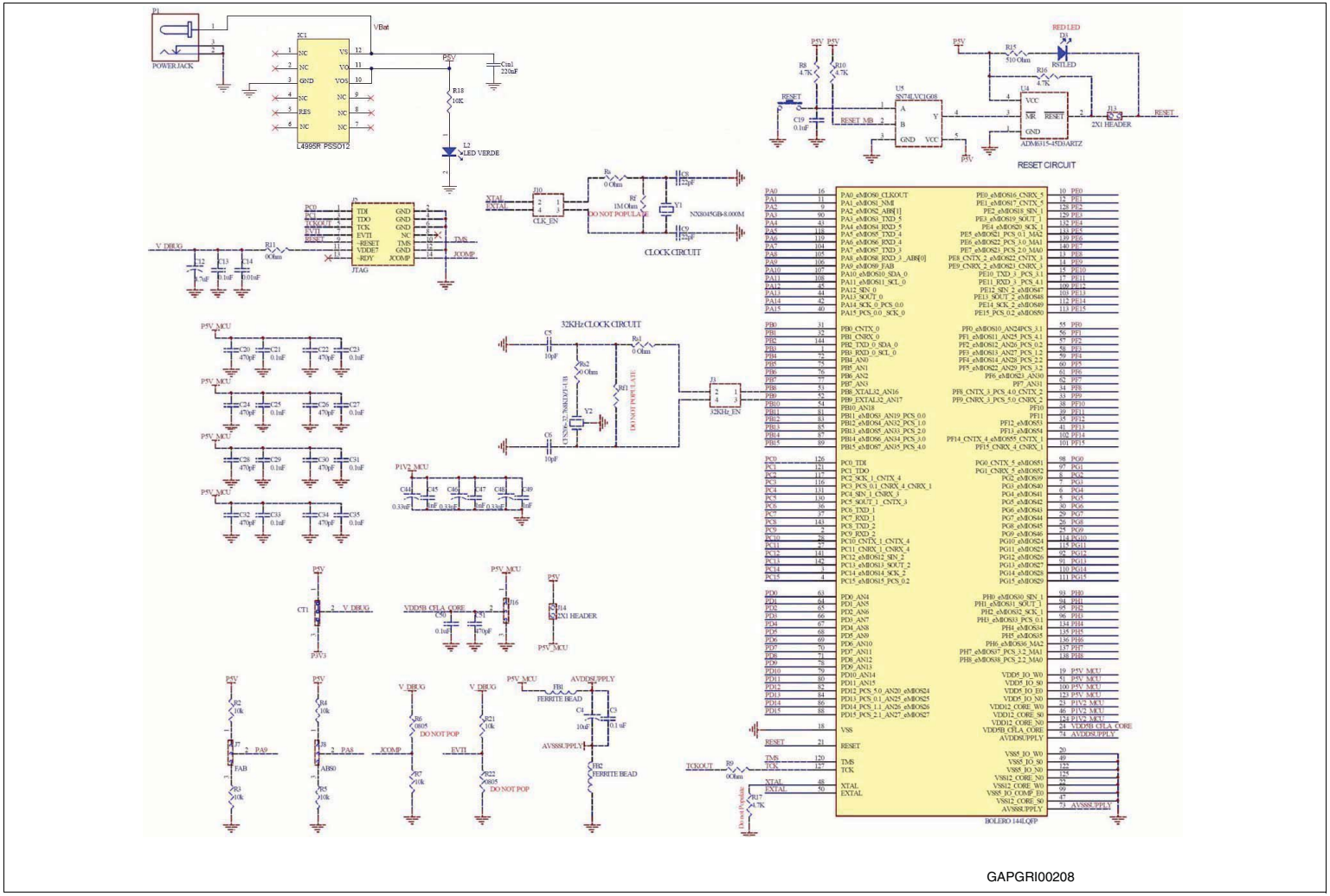
  Usually in a system it is possible identify different parts of circuits including digital, analog, high current switching circuitry, I/O, and the main power supply. If these different parts of the circuit use isolated grounds, they will be connected together at a single point.

- PCB considerations:
  - For single-chip applications, a minimum of four layers is used. For expanded mode applications, a minimum of six layers is used.
  - There is at least one ground plane.
  - There is at least one power plane.
  - From the power and ground planes have not be present structures which obstruct the flow of current, such as via overlapping (it is not allowed three via anti-pads to merged). Furthermore, vias should be staggered as much as possible because aligned vias create slots that obstruct the flow of current.

9 Reference schematic

Figure 15 shows a typical application schematic.

Figure 15. Typical application schematic



Appendix A Document management

A.1 Reference documents

- *SPC560B4x, SPC560B5x, SPC560C4x, SPC560C5x 32-bit MCU family built on the embedded Power Architecture®* (reference manual RM0017, Doc ID 14629)
- *32-bit MCU family built on the Power Architecture® embedded category for automotive body electronics applications* (SPC560B4x, SPC560B5x, SPC560C4x, SPC560C5x datasheet, Doc ID 14619)
- *32-bit MCU family built on the Power Architecture® embedded category for automotive body electronics applications* (SPC560B4x/50 – SPC560C4x/50 errata sheet, Doc ID 15844)

A.2 Acronyms

Table 5. Acronyms

Acronym	Name
ADC	Analog-to-digital converter
BAM	Boot assist mode
CRC	Cyclic redundancy check
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESL	Equivalent series inductance
ESR	Equivalent series resistance
LVD	Low voltage detector
NVUSRO	Non-volatile user options register
POR	Power-on reset
SIUL	System integration unit lite
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Revision history

Table 6. Document revision history

Date	Revision	Changes
22-Sep-2009	1	Initial release.
03-Sep-2010	2	Editorial and formatting changes throughout document Updated *Section 1.3: Current consumption and voltage regulator* and *Section 7.5: I/O characteristic in STANDBY mode* Added *Section 8: EMC guidelines* Updated *Table 5: Acronyms*
04-Jun-2012	3	Added *Section 4.3.1: Some recommended crystal*.

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